Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VIN**
2. **GND**
3. **VOUT**
4. **VOUT**

**.055”**

**4**

**3**

**1**

**2**

**MASK**

**REF**

**EH7812**

**.075”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .008 x .008”**

**Backside Potential: GND**

**Mask Ref: EH7812**

**APPROVED BY: DK DIE SIZE .055” X .075” DATE: 1/30/23**

**MFG: SILICON SUPPLIES THICKNESS .011” P/N: 7812AC**

**DG 10.1.2**

#### Rev B, 7/1